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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/429,283	10/28/99	UENO	S 0057-2534-2Y

EXAMINER	
FOURSON, III, G	
ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/429,283	UENO ET AL.	
	Examiner	Art Unit	
	George Fourson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☒ The proposed drawing correction filed on *28 October 1999* is: a)☒ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/958,546* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

The finality of the office action mailed 2/13/01 and the indicated allowability of claims 17,18 and 19-27 is withdrawn in view of the new grounds of rejection below.

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 14-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Japanese Patent 4-157766, Gardner et al '849, Choi '330, Chou et al (1997 IEEE) and Kuroi et al (J. Appl. Phys. 1995).

3. Japan '766 discloses formation of a field oxide isolated P-channel transistor including selective implantation of nitrogen into the polysilicon layer later patterned to form the gates of a p-channel transistor having nitrogen in the lower portion of the gate and an n-channel transistor having no nitrogen in the gate (abstract and figures 1A-1C).

4. Choi discloses blanket p-type doping of a polysilicon layer 200 followed by selective doping of layer 200 in region 112 such that the gates of all transistors formed in region 112 would contain p-type dopant due to the blanket implantation (fig 3a-3c). The reference discloses that nitrogen implantation can be combined with such a process (col.8, lines 16-18).

5. Gardner et al discloses the dependence of threshold voltage on concentration of dopant in the gate of a MOSFET and the formation of MOSFET's having different concentrations of dopant on the same wafer (col.10, lines 19-26 and col.12, lines 1-11).

6. Chou et al discloses the effects of different concentrations of nitrogen in the gate of a MOSFET with respect to type of dopant (Chou et al, introduction).

7. Kuroi et al discloses the effects of different nitrogen concentrations and dopant concentrations in the gate of a MOSFET (see Fig.2 and 3).

8. It would have been within the scope of one of ordinary skill in the art to combine Japanese Patent 4-157766 and Choi '330 to enable doping of the polysilicon layer of Japan '766 in the p-channel area and to further combine the teachings of the references with those of Gardner et al to enable formation of circuits having a desired characteristic as disclosed by Gardner. The choice of particular dopant and nitrogen concentrations in the gates of the MOSFET's so produced, including formation of MOSFET's having more than 2 different concentrations of nitrogen would have been a matter of routine optimization in view of the teachings of Chou et al and Kuroi et al that these are result effective variables and in view of Gardner that the choice depends on the desired device characteristics. Furthermore, the claims are open to the amounts of dopant in the gates differing to an extent that is insufficient to substantially alter the device performance as compared to a device having all gates doped equally.

9. The examiner takes official notice that formation of a capacitor connected to a source/drain region of a MOSFET was known at the time of applicant's invention in formation of DRAM's. It would have been within the scope of one of ordinary skill in the art to combine the known process with that made obvious by the combination of references discussed above to enable DRAM formation.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956. See MPEP 203.08.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner George Fourson whose telephone number is (703) 308-2544. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax number for this group is (703)308-7722(7724,3431 and 3432). MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

George Fourson
Primary Examiner
Art Unit 2823

GFourson
June 12, 2001